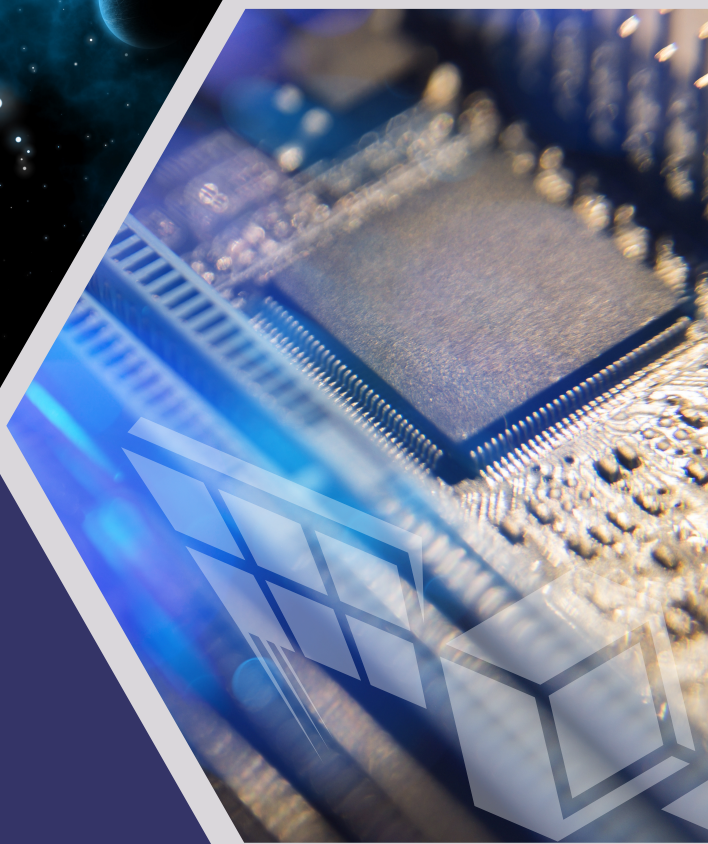
De-RISC

Dependable Real-time Infrastructure for Safety-critical Computer

The first RISC-V, fully European platform for space



RISC-V multi-core platform and hypervisor for time and space isolation for applications within space and aeronautical domains.

www.derisc-project.eu

Requirements → Implementation → Validation

- No US export restriction
- Multi-core interference mitigation
- Portability
- Fault-tolerance
- Open standards

GOALS

1. Strengthen European leadership in the supply of Integrated Modular Avionics HW/SW.
2. Consolidate the European position in real-time embedded processors technology.
3. Capitalize on the economy of scale by reinforcing an open standard Instruction Set Architecture (ISA) for the embedded market.

H2020 De-RISC

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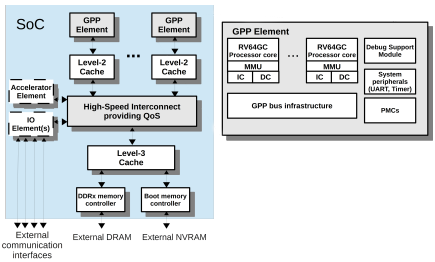
De-RISC will deliver a complete stack with a fault-tolerant RISC-V multi-processor system-on-chip (MPSoC) design together with qualified hypervisor software, available for use on a CPCI Serial Space development board.

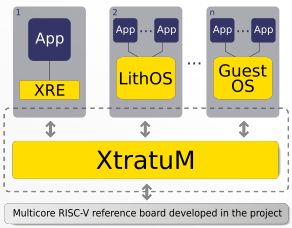
Hardware development

On the hardware side, De-RISC will integrate an MPSoC composed of NOEL-V cores from Cobham Gaisler including safety-critical hardware support (monitoring units and contention control) by Barcelona Supercomputing Center, ready for space applications providing them with the required level of performance.



Software development

On the software side, De-RISC will provide the XtratuM hypervisor from Fent Innovative Software Solutions (fentISS) and a representative modular application from Thales Research & Technology.



fentISS · Barcelona Supercomputing Center · THALES · CAES PIONEERING ADVANCED ELECTRONICS

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